REMARKS

Claims 1 and 3-16 are all of the claims pending in the application.

IDS and Drawings:

Applicants again note that they have not received an initialed copy of Form PTO 1449, filed on April 27, 2000, and request the Examiner to provide an initialed copy in the next Patent Office paper.

35 U.S.C. §102(b) - claims 1, 3-6 and 8:

Claims 1, 3-6, 8, 13 and 15 are rejected under 35 U.S.C. §102(b) as being anticipated by Pakeriasamy (U.S. Pat. No. 5,957,293).

The Examiner alleges that Pakeriasamy discloses the elements of claim 1. In an attempt to explain this assertion, the Examiner provides a modified sketch of Figure 7 of Pakeriasamy (see Office Action, page 2, section 2). The Examiner labels this sketch as having a first area and a second area. The first area represents a side of an indentation, and the second area represents a lip of the indentation. An electronic package is shown as being in contact with the first area.

Applicants respectfully submit that rejections under 35 U.S.C. §102 are proper only when each element of the claimed subject matter is disclosed in the cited reference, and that Pakeriasamy fails to disclose each element of the claims.

Specifically, claim 1 recites, *inter alia*:

"...said first wall surface being inclined at an angle so as to support an edge of the package of the semiconductor integrated circuit device such that the wiring terminals of the semiconductor integrated circuit device do not contact said first wall surface when the semiconductor integrated circuit device is stored in said first storage portion..."

Specifically, claim 1 describes that when the semiconductor integrated circuit device is stored in the first storage portion, the wiring terminals of the semiconductor integrated circuit device do not contact the first wall surface. Contact is further prohibited even when the semiconductor integrated circuit device is inclined such that a side of the device rests on an upper edge of the first wall surface and the other side rests on a portion of the first wall surface below the upper edge. This feature is not described in Pakeriasamy.

Claim 1 further recites, *inter alia*:

"*a first wall surface* extending from said bottom surface...

a second wall surface disposed around a *circumference of the semiconductor integrated circuit device* so as to limit horizontal movement of the semiconductor integrated circuit device,...

said second wall surface *extending from* said first wall surface *in a direction away* from said first wall surface of said main body..." (Emphasis added.)

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The portions of Pakeriasamy that the Examiner labeled as the first and second areas, fail to disclose at least these recitations. Specifically, claim 1 describes the second wall surface as extending away from the first wall surface, and the second wall surface as being disposed around a circumference of the semiconductor integrated circuit device so as to limit horizontal movement of the circuit device.

However, the Examiner's analysis of figure 7 of Pakeriasamy does not meet the claimed recitations because the second area, as labeled by the Examiner, is not disposed around a circumference of the circuit device so as to limit horizontal movement of the device. Instead the second area of Pakeriasamy is under a corner of an indentation. However, this corner is not disposed around a circumference of the electronic device, but is rather positioned above and beyond the device, and not in an area which allows for it to limit horizontal movement of the device. The area of Pakeriasamy which contacts the device is the first area, as labeled by the Examiner; however, this first area does not have a second wall surface extending from it which is disposed around the circumference of the circuit device. This is because the first area, as labeled by the Examiner, is shown to be of a consistent angle, and because it is formed to be of a consistent angle, it is not capable of being broken up into a first wall surface and a second wall surface, which respectively extend away from each other, as in a claimed embodiment of the present invention.

Additionally, Applicants submit that even if the Examiner alters the sketch of Figure 7 by showing the first area as being towards the very bottom of the side wall of the indentation, as opposed to the middle, the recitations of the claims are still not met. This is because claim 1

recites the first wall surface as being arranged around the semiconductor integrated circuit device. However, the bottom portion of the side wall of Pakeriasamy is not arranged around any portion of the circuit device, but is clearly positioned below and beneath the circuit device. Thus, each and every element of the claimed subject matter is not taught by Pakeriasamy, nor are the claimed elements suggested by this reference.

Consequently, claim 1 cannot be anticipated by Pakeriasamy, and the rejection of claim 1 under 35 U.S.C. §102(b) should be withdrawn.

Dependent claims 1, 3-6 and 8 also are not anticipated by Pakeriasamy, at least by virtue of their respective dependencies on independent claim 1.

35 U.S.C. §102(b) - claims 13 and 15:

Applicants respectfully submit that Pakeriasamy also fails to teach the recitations of claims 13 and 15. Specifically, claims 13 recites, *inter alia*:

> "...wherein when two of said trays are aligned in a stacked relationship ... and when said two aligned trays are not turned over, the *one of said two trays which is positioned on top, does not make contact* with a *stored semiconductor integrated circuit device.*" (Emphasis added.)

Pakeriasamy does not teach at least these recitations. In contradistinction, Pakeriasamy actually teaches away from these recitations. This is because Pakeriasamy teaches the use of a top tray which clearly contacts a circuit device disposed in a bottom tray, as shown in Figure 7.

Thus, when two trays of Pakeriasamy are aligned in a stacked relationship and are not turned over, as in Figure 7, the one of the two trays which is positioned on top, does make contact with the stored semiconductor integrated. Accordingly, the recitations of claim 13 are not taught by Pakeriasamy, nor would one skilled in the art have found such recitations obvious in light of the reference.

Applicants also submit that claim 15 is allowable at least by virtue of its dependency on claim 13, in addition to its individual recitations.

35 U.S.C. §103(a) - claims 7, 9, 14 and 16:

The Examiner asserts that claims 7, 9 and 14 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pakeriasamy in view of Nemoto (U.S. Pat. No 5,418,692).

In regard to claims 7 and 9, Applicants submit that since claims 7 and 9 respectively depend upon claim 1, and since Nemoto does not cure the deficient teachings of Pakeriasamy with respect to claim 1, claims 7 and 9 are patentable at least by reason of their dependencies, in addition to their individual recitations.

In regard to claims 14 and 16, Applicants submit that since claims 14 and 16 respectively depend upon claim 13, and since Nemoto does not cure the deficient teachings of Pakeriasamy with respect to claim 13, claims 14 and 16 are patentable at least by reason of their dependencies, in addition to their individual recitations.

In regard to claim 13, the reason that Nemoto does not cure the deficient teachings of Pakeriasamy is because that Nemoto actually teaches away from the claimed recitations. This teaching away is made apparent by the Examiner's statement on page 3, section 4, where it is

stated that "Nemeto suggests providing a second storage pocket as shown in Figure 8b wherein the angled protruding portions engage both the top surface and the corner of a component to stabilize the component and prevent movement vertically and horizontally." (Emphasis added.) In light of this disclosure, one skilled in the art would not have gleaned the recitations of claim 13 which include that "one of said two trays which is positioned on top, does not make contact with the stored semiconductor integrated circuit device." (Emphasis added.)

35 U.S.C. §103(a)- claims 10-12:

Claims 10-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Pakeriasamy. Accordingly, Applicants submit that since claims 10-12 respectively depend upon claim 1, and the Examiner's current application of Pakeriasamy does not cure the deficient teachings of the original application of Pakeriasamy with respect to claim 1, claims 10-12 are patentable at least by reason of their dependencies, in addition to their individual recitations.

Reconsideration and allowance of all claims are respectfully requested in view of the preceding remarks. In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

Applicants hereby petition for any extension of time that may be required to maintain the pendency of this case, and any required fee (except for the Issue Fee) is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Twice Amended) A tray for storing a semiconductor integrated circuit device having a package and wiring terminals on a lower surface of the package, said tray comprising:

a substantially planar main body; and

a first storage portion provided on a first surface of said main body for storing the semiconductor integrated circuit device, said first storage portion having a bottom surface and a first wall surface ~~adapted to be~~ extending from said bottom surface and arranged around the semiconductor integrated circuit device when the semiconductor integrated device is stored in said first storage portion,

~~wherein said first wall surface has a first area and~~ a second wall surface ~~area,~~ disposed around a circumference of the semiconductor integrated circuit device so as to limit horizontal movement of the semiconductor integrated circuit device, said first ~~area~~ wall surface being inclined at an angle so as to support an edge of the package of the semiconductor integrated circuit device such that the wiring terminals of the semiconductor integrated circuit device do not contact ~~and to prevent~~ said first wall surface ~~from coming into contact with the wiring terminals~~

~~of the semiconductor integrated circuit device~~ when the semiconductor integrated circuit device is stored in said first storage portion, and said second ~~area~~ wall surface extending from said first wall surface ~~area~~ in a direction away from said first wall surface of said main body, wherein said second wall surface ~~area~~ is inclined at an angle larger than the angle of said first ~~area~~ wall surface, with respect to the horizontal.

13. (Amended) A tray for storing a semiconductor integrated circuit device having a package and wiring terminals on a lower surface of the package, said tray comprising:

a substantially planar main body;

a first storage portion provided on a first surface of said main body for storing the semiconductor integrated circuit device, said first storage portion having a first wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated device is stored in said first storage portion, wherein said first wall surface has a first area which is inclined at an angle so as to support an edge of the package of the semiconductor integrated circuit device and to prevent said first wall surface from coming into contact with the wiring terminals of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion; and

a second storage portion provided on a second surface of said main body opposite to said first storage portion, wherein said second storage portion can store a semiconductor integrated circuit device with wiring terminals thereof facing upward when said tray is turned over, and

wherein when two of said trays are aligned in a stacked relationship said second storage portion of one tray cooperates with said first storage portion of the other tray to form a space for storing the semiconductor integrated circuit device, ~~wherein when two of said trays are aligned in a stacked relationship, said second storage portion of one tray cooperates with said first storage portion of the other tray to form a space for storing the semiconductor integrated circuit device~~ and when said two aligned trays are not turned over, the one of said two trays which is positioned on top, does not make contact with a stored semiconductor integrated circuit device.

16. (Amended) A tray according to claim 13, wherein said main body includes a plurality of projecting pieces provided on said second surface thereof for defining said second storage portion, and wherein each of said projecting pieces has a wall surface for serving as said second wall surface, whereby said wall surfaces of said projecting pieces respectively support corners of the rectangular package of the semiconductor integrated circuit device, when said tray is in a turned-over state.